XILINX FPGA

VIVADO DESIGN SUITE

TRAINING	PRICE	SESSIONS
F_VBASE Designing FPGAs Using the Vivado Design Suite (3d)	2200 €	• Oct 09, 2019 SEVRES(92)
F_STAXDC Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and UltraFast Design Methodology (3d)	2200 €	• Dec 02, 2019 PLAISANCE(31)
F_VADV Advanced use of the Vivado Design Suite (3d)	On site and/or according to requests	
F_PR Partial Reconfiguration (2d)	1600 €	• Dec 05, 2019 SEVRES(92)

ARCHITECTURE ADVANCED TRAINING

TRAINING	PRICE	SESSIONS
F_US Designing with the Xilinx™ UltraScale and UltraScale+ Families (2d)	1600 €	
F_7SERIE Designing with the Xilinx™ 7-Series Families (2d)	On site and/or according to requests	
F_V6 Designing with the Virtex-6 Family (2d)	On site and/or according to requests	
F_S6 Designing with the Spartan-6 Family (2d)	On site and/or according to requests	

XILINX SOC & MPSOC

SOC ZYNQ-7000®

TRAINING	PRICE	SESSIONS
E_ZAHS The essentials of embedded design for Xilinx components (4d)	3200 €	• Sep 30, 2019 SEVRES(92)
E_ZADV Zynq™ : Embedded Systems Advanced Design (2d)	1600 €	
E_ZSA Zynq™ : System Architecture (2d)	On site and/or according to requests	
E_HW Zynq™ : Embedded Systems Hardware Design (2d)	On site and/or according to requests	
E_SW Zynq™ : Embedded Systems Software Design (2d)	On site and/or according to requests	

MPSOC ZYNQ® ULTRASCALE+™

TRAINING	PRICE	SESSIONS
E_ZUPSA Zynq UltraScale+™ MPSoC : System Architecture (2d)	2000 €	
E_ZUPSW Zynq UltraScale+™ MPSoC : Hardware and Software Design (2d)	2000 €	

ADVANCED TOOLS

TRAINING	PRICE	SESSIONS
SDSoC™		
E_SDSOCx SDSoC Development Environment and Methodology and Advanced Training (2 in 1) (3d)	2500 €	
E_SDSOC SDSoC Development Environment and Methodology (1d)	1200 €	
E_ADVSDS Advanced SDSoC Development Environment and Methodology (2d)	2000 €	
Vivado™ HLx		
D_HLS Vivado™ High Level Synthesis (2d)	1600 €	• Nov 12, 2019 SEVRES(92)
PetaLinux™		
E_PLNX Embedded Design with Xilinx™ PetaLinux Tools (2d)	2000 €	• Sep 26, 2019 PLAISANCE(31)

CONNECTIVITY

MULTI-GIGABIT TRANSCEIVERS

TRAINING	PRICE	SESSIONS
C_TRX Designing with Xilinx Serial Transceivers (2d)	1600 €	• Oct 17, 2019 SEVRES(92)

PCI EXPRESS

TRAINING	PRICE	SESSIONS
C_PCIE Designing a LogiCore PCI Express system (2d)	On site and/or according to requests	

ETHERNET

TRAINING	PRICE	SESSIONS
003368A Ethernet Bus (2d)	On site and/or according to requests	
003367A Ethernet & Switching (4d)	On site and/or according to requests	

DIGITAL SIGNAL PROCESSING ON FPGA

DSP FUNCTIONS

TRAINING	PRICE	SESSIONS
D_ESS Essential DSP implementation techniques for Xilinx™ FPGAs (2d)	On site and/or according to requests	

HDL LANGUAGES

VHDL

TRAINING	PRICE	SESSIONS
L_VHDL VHDL Logical Synthesis and Simulation for Xilinx™ FPGA design (5d)	2500 €	• Nov 25, 2019 SEVRES(92)