Workshop : Getting Started with Xilinx Versal ACAP Platform (French Language)

1 day - 7 hours

OBJECTIVES

- In the Event, you will be introduced to the new Xilinx Versal ACAP platform and its building blocks that enable flexible implementation of accelerated systems. Features unique to Versal, such as the AI Engine and Network-on-Chip (NoC) along with the Vitis Unified Software tool flows will be covered. The objective is to let you relate your new applications to Versal and enable you to explore the platform and the tools.

RELATED TRAININGS

- Designing with the Versal ACAP: Architecture and Methodology and NoC
- Designing with Versal™ AI Engine

PREREQUISITES

- Comfort with the C/C++ programming language
- Vitis™ IDE software development flow
- Hardware development flow with the Vivado® Design Suite
- Basic knowledge of UltraScale™/UltraScale+™ FPGAs and Zynq® UltraScale+ MPSoCs

PARTNERS

XILINX® | Authorized Training Provider

CONFIGURATIONS

- Software Configuration :
  - Vitis unified software platform 2021.1
  - PetaLinux 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS 64-bits (Ubuntu, RedHat, Centos)
  - At least 16GB RAM
  - Recommended display resolution 1920x1080

CHAPTERS

DAY 1

- Architecture Overview
- Design Tool Flow
- Processing System
- NoC Introduction and Concepts
- AI Engine
- SelectIO Resources
- System Simulation
- Application Partitioning

TEACHING METHODS

- Inter-company training:
  - Onlive training
  - Presentation by Webex
  - Provision of PDF course materials

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA/SoC/MPSoC/RFSoC/ACAP XILINX - Languages VHDL/Verilog - DSP - Design RTL - Embedded C

CONCERNED PUBLIC

- Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Xilinx Versal ACAP device

CONTACT

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