Upgrading VHDL to Verilog and Verilog to VHDL

2 days - 14 hours

OBJECTIVES

- After completing this training, you will have the skills to:
  - 1 - Know the instruction sets for RTL synthesis and grasp the differences and the multiple possibilities offered by the VHDL and Verilog languages
  - 2 - Know the instruction sets for the simulation and grasp the differences and the multiple possibilities offered by the VHDL and Verilog languages

PREREQUISITES

- This course is intended for electronic engineers who already have a good knowledge of digital electronic circuit design, and who master one of the RTL logic synthesis languages (VHDL or Verilog), and who wish to acquire additional knowledge of the second RTL logic synthesis language (VHDL or Verilog).

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 13/12/2021

CHAPTERS

DAY 1

- Objective 1
  - Rules for writing VHDL/Verilog code in logical synthesis
    - Concept of entity/architecture
    - Predefined objects and types
    - Competing Instructions
    - Sequential instructions
  - Hierarchy management for better reuse
    - Notions of variables and examples of use
    - Generality and automatic parameterization of reusable modules
    - Predefined Attributes Useful in Logical Synthesis
    - Functions and procedures
    - Definition of packages and libraries

DAY 2

- Objective 2
  - Testbenches and simulation
    - Some basic rules for writing an efficient testbench
    - Simulation-specific instructions
    - Writing component models to make simulation more realistic
    - Writing and reading ASCII files
    - Generation of information messages

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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La certification a été délivrée au titre de la catégorie d'action suivante :
ACTIONS DE FORMATION