Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and Advanced use of Vivado

4 days - 28 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Describe the UltraFast™ design methodology checklist
  - 2 - Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
  - 3 - Master the software flow in order to know the possibilities of the Vivado tool
  - 4 - Apply exhaustive design constraints (XDC) including timing exceptions, and use appropriate timing reports to locate critical paths
  - 5 - Identify key areas to optimize your design, minimize metastability issues and make your system reset more reliable
  - 6 - Apply advanced I/O timing constraints to meet performance goals
  - 7 - Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode
  - 8 - Utilize floorplanning techniques to improve design performance
  - 9 - Debugging a design during the start-up phase and using the advanced debugging functions

PREREQUISITES

- Intermediate knowledge in HDL language and a first experience with the Vivado™ Design suite and FPGAs.

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 20/12/2021

CHAPTERS

DAY 1

- Objective 1
  - Introduction to FPGA Architecture, 3D ICs, SoCs {Lecture}
  - UltraFast Design Methodology: Board and Device Planning {Lecture}
  - UltraFast Design Methodology: Design Creation {Lecture}
- Objective 2
  - HDL Coding Techniques {Lecture}
  - Pipelining {Lecture}
  - Inference {Lecture}
- Objective 3
  - Vivado Design Suite Flows {Lecture, Labs}
  - Scripting in Vivado Design Suite {Lecture}
  - Vivado Synthesis and Implementation {Lecture, Lab}
  - UltraFast Design Methodology: Implementation {Lecture}
  - Introduction to Vivado Reports {Lecture}
  - Design Analysis using Tcl Commands {Lecture}

DAY 2

- Objective 4
  - Baselining {Lecture}
  - Timing Constraints Editor {Lecture}
  - Timing Summary Report {Lecture}
  - Clocking Resources {Lecture}
  - Introduction to Clock Constraints {Lecture}
  - Generated Clocks {Lecture, Lab}
  - Report Clock Networks {Lecture}
  - Clock Group Constraints {Lecture}
  - Report Clock Interaction {Lecture}
  - Setup and Hold Timing Analysis {Lecture}
  - I/O Constraints and Virtual Clocks {Lecture, Lab}
  - Timing Constraints Wizard {Lecture}
  - Introduction to Timing Exceptions {Lecture, Lab}

DAY 3

- Objective 5
  - Synchronous Design Techniques {Lecture}
  - Synchronization Circuits {Lecture, Lab}
  - Resets {Lecture}
  - Register Duplication {Lecture}
  - Report QoR {Lecture}
  - UltraFast Design Methodology: Design Closure {Lecture}
- Objective 6
  - Report Datasheet {Lecture}
  - I/O Timing Scenarios {Lecture}
  - System-Synchronous I/O Timing {Lecture}
  - Source-Synchronous I/O Timing {Lecture, Lab}
  - I/O Logic Resources {Lecture}
  - Timing Constraints Priority {Lecture}
- Objective 7
  - Physical Optimization {Lecture, Lab}

DAY 4

- Objective 7
  - Incremental Compile Flow {Lecture, Lab}
  - Vivado Design Suite ECO Flow {Lecture, Lab}
  - Congestion {Lecture}
- Objective 8
  - Introduction to Floorplanning {Lecture}
  - Design Analysis and Floorplanning {Lecture, Lab}
- Objective 9
  - JTAG to AXI Master Core {Lecture}
  - Remote Debugging Using the Vivado Logic Analyzer {Lecture}
  - Trigger and Debug at Device Startup {Lecture}
  - Trigger Using the Trigger State Machine in the Vivado Logic Analyzer {Lecture, Lab}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
    - Technical questionnaire
    - Result of the Practical Works
    - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

CONTACT

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