Designing FPGAs Using the Vivado™

4 days - 28 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Use the Vivado IDE I/O Planning layout to perform pin assignments
  - 2 - Describe the supported design flows of the Vivado IDE
  - 3 - Synthesize and implement the HDL design, and generate a DRC report to detect and fix design issues
  - 4 - Create and package your own IP and use the Vivado IP integrator to create a block design
  - 5 - Describe how power analysis and optimization is performed
  - 6 - Apply clock, I/O timing and timing exception constraints and perform timing analysis
  - 7 - Identify synchronous design techniques
  - 8 - Describe how the FPGA is programmed
  - 9 - Use the Vivado logic analyzer and debug cores to debug a design

PREREQUISITES

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 20/12/2021

CHAPTERS

DAY 1

- Objective 1
  - Introduction to Vivado Design Flows {Lecture}
  - Introduction to FPGA Architecture, 3D IC, SoC {Lecture}
  - UltraFast Design Methodology: Planning {Lecture}
  - Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Objective 2
  - Vivado Design Suite Project Mode {Lecture, Lab}
  - Scripting in Vivado Design Suite Project Mode {Lecture}
  - UltraFast Design Methodology: Design Creation and Analysis {Lecture}
  - HDL Coding Techniques {Lecture}
  - Inference {Lecture}
  - Simulation {Lecture, Lab}
- Objective 3
  - Synthesis and Implementation {Lecture, Lab}
  - Introduction to Vivado Reports {Lecture, Labs}

DAY 2

- Objective 4
  - Vivado IP Flow {Lecture, Lab}
  - Creating and Packaging Custom IP {Lecture, Lab}
  - Using an IP Container {Lecture}
  - Designing with IP Integrator {Lecture, Lab}
- Objective 5
  - Power Analysis and Optimization Using the Vivado Design Suite {Lecture}
- Objective 6
  - Baselining {Lecture}
  - Timing Constraints Editor {Lecture}
  - Timing Summary Report {Lecture}
  - Clocking Resources {Lecture}
  - Introduction to Clock Constraints {Lecture}

DAY 3

- Objective 6
  - Generated Clocks {Lecture, Lab}
  - Report Clock Networks {Lecture}
  - Clock Group Constraints {Lecture}
  - Report Clock Interaction {Lecture}
  - Setup and Hold Timing Analysis {Lecture}
  - I/O Logic Resources {Lecture}
  - I/O Constraints and Virtual Clocks {Lecture, Lab}
  - Timing Constraints Wizard {Lecture}
  - Introduction to Timing Exceptions {Lecture, Lab}
- Objective 7
  - Synchronous Design Techniques {Lecture}
  - Synchronization Circuits {Lecture}
  - Timing Constraints Priority {Lecture}

DAY 4

- Objective 8
  - Introduction to FPGA Configuration {Lecture}
  - Configuration Process {Lecture}
  - Configuration Modes {Lecture}
  - Daisy Chains and Gangs in Configuration {Lecture}
  - Bitstream Security {Lecture}
- Objective 9
  - Introduction to the Vivado Logic Analyzer {Lecture}
  - Introduction to Triggering {Lecture}
  - Debug Cores {Lecture}
  - HDL Instantiation Debug Probing Flow {Lecture, Lab}
  - Netlist Insertion Debug Probing Flow {Lecture, Lab}
  - Debug Flow in an IP Integrator Block Design {Lecture, Lab}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:

    - Technical questionnaire
    - Result of the Practical Works
    - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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