Designing with Dynamic Function eXchange (DFX) Using the Vivado Design Suite

3 days - 21 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Describe what Dynamic Function eXchange is, and the DFX tool flow with Vivado
  - 2 - Identify how Dynamic Function eXchange affects various resources for Xilinx Devices
  - 3 - Use the block design container feature of Vivado IP integrator to create a DFX design
  - 4 - Generate the appropriate full and partial bitstreams for a DFX design
  - 5 - Implement and debug a Dynamic Function eXchange system
  - 6 - Implement a DFX system in an embedded environment using the Vitis IDE

PREREQUISITES

- Designing FPGAs with the Vivado Design Suite course
- Working HDL knowledge (VHDL or Verilog)

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 20/12/2021

CHAPTERS

DAY 1

- Objective 1
  - Introduction to Dynamic Function eXchange (DFX) {Lecture}
  - DFX Flow Using the Vivado Design Suite GUI {Lecture, Lab}
  - DFX Flow Using Vivado Design Suite Tcl Commands {Lecture, Lab}
  - Nested DFX {Lecture, Lab}
  - Abstract Shell for Dynamic Function eXchange {Lecture}

DAY 2

- Objective 2
  - DFX Design Considerations for All Xilinx Devices {Lecture}
  - DFX Design Considerations for 7 Series, Zynq SoC, UltraScale, and UltraScale+ Devices {Lecture}
  - DFX Design Considerations for Versal Devices {Lecture}
- Objective 3
  - DFX Intellectual Property (IP) {Lecture, Lab}
  - DFX Block Design Containers in IP Integrator {Lecture, Lab}
- Objective 4
  - Configuring Devices Using DFX {Lecture}
  - Configuration Parameters {Lecture}
  - DFX Bitstreams {Lecture}
  - DFX Bitstream Integrity {Lecture}

DAY 3

- Objective 5
  - Floorplanning a DFX Design {Lecture, Lab}
  - DFX Timing Analysis and Constraints {Lecture, Lab}
  - DFX Debugging {Lecture, Lab}
- Objective 6
  - DFX in Embedded Systems {Lecture, Lab}
  - DFX Designs Using the PCIe Core {Lecture}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vitis 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

XILINX | Authorized Training Provider

CONTACT

Administratif : +33 (0)6 30 94 50 17
Formateur : +33 (0)6 74 52 37 89
info@mvd-training.com

DATADOCKÉ