Designing with the Xilinx™ 7-Series Families

2 days - 14 hours

OBJECTIVES

- After completing this comprehensive training, you will have the necessary skills to:
  - Describe all the functionality of the 6-input LUT and the CLB construction of the 7 series FPGAs
  - Specify the CLB resources and the available slice configurations for the 7 series FPGAs
  - Define the block RAM, FIFO, and DSP resources available for the 7 series FPGAs
  - Properly design for the I/O block and SERDES resources
  - Identify the MMCM, PLL, and clock routing resources included with these families
  - Identify the hard resources available for implementing high performance DDR3 physical layer interfaces
  - Describe the additional dedicated hardware for all the 7 series family members
  - Properly code your HDL to get the most out of the 7 series FPGAs

RELATED TRAININGS

- Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and Advanced use of Vivado
- The essentials of embedded design for Xilinx Zynq™-7000 & Zynq MPSoC components

PREREQUISITES

- Basic knowledge FPGAs architectures
- A successful first experience of designing an VHDL–based FPGA

PARTNERS

XILINX | Authorized Training Provider

CONFIGURATIONS

- Software Configuration :
  - Vivado Design Suite 2020.2
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

CHAPTERS

DAY 1

- 7 Series FPGA Overview
- CLB Architecture
- Slice Flip-Flops
- Lab 1: CLB Resources
- Memory Resources
- Lab 2: Memory Resources
- DSP Resources
- Lab 3: DSP Resources

DAY 2

- I/O Resources
- Lab 4: I/O Resources
- Clocking Resources
- Lab 5: Clocking Resources
- Memory Controllers
- Dedicated Hardware
- Coding Techniques

TEACHING METHODS

- Classroom training:
  - Face to face
  - Presentation by video projector
  - Provision of PDF course materials
- Virtual training:
  - Onlive training
  - Presentation by Webex
  - Provision of PDF course materials

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics

CONTACT

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