# Zynq UltraScale+™ MPSoC : System Architecture, Hardware and Software Design

4 days - 28 hours

## OBJECTIVES

- After completing this training, you will have the skills to:
  - 1 - Outline the high-level architecture of the devices
  - 2 - Define the underlying implementation of the application processing unit (APU) and real-time processing unit (RPU) to make best use of their capabilities
  - 3 - Effectively use power management strategies and leverage the capabilities of the platform management unit (PMU)
  - 4 - Identify mechanisms to secure and safely run the system
  - 5 - Define boot sequences appropriate to the needs of the system
  - 6 - Identify situations when a hypervisor should be used
  - 7 - Distinguish between asymmetric multiprocessing (AMP) and symmetric multiprocessing (SMP) environments

## PREREQUISITES

- Understanding of the Zynq™-7000 architecture
- Familiarity with embedded operating systems

## CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

## NOTES

- Release date: 20/12/2021

## CHAPTERS

**DAY 1**

- Objective 1
  - Zynq UltraScale+ MPSoC Overview {Lecture, Lab}
- Objective 2
  - Zynq UltraScale+ MPSoC Application Processing Unit {Lecture, Lab}
  - Zynq UltraScale+ MPSoC Real-Time Processing Unit {Lecture, Lab}
  - Zynq UltraScale+ MPSoC DDR and QoS {Lecture, Lab}
  - Zynq UltraScale+ MPSoC System Coherency {Lecture}
  - QEMU {Lecture, Lab}

**DAY 2**

- Objective 3
  - Zynq UltraScale+ MPSoC Power Management {Lecture, Lab}
  - Zynq UltraScale+ MPSoC PMU {Lecture, Lab}
- Objective 4
  - Zynq UltraScale+ MPSoC Security and Software {Lecture}
  - Zynq UltraScale+ MPSoC System Protection {Lecture}
  - ARM TrustZone Technology {Lecture}

**DAY 3**

- Objective 5
  - Zynq UltraScale+ MPSoC Booting {Lecture, Lab}
- Objective 6
  - MultiProcessor Software Architecture {Lecture}
  - Zynq UltraScale+ MPSoC HW-SW Virtualization {Lecture}
  - Xen Hypervisor {Lecture} (pairs with OpenAMP, but not SMP)

**DAY 4**

- Objective 7
  - OpenAMP {Lecture} (pairs with the Xen Hypervisor, but not SMP)
  - Linux {Lecture}
  - Yocto {Lecture}
  - Open Source Library (Linux) {Lecture, Lab}
  - FreeRTOS {Lecture, Lab}

## TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

## METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

## SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

## PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vitis 2021.1
  - Petalinux 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

## PARTNERS

AMD
Authorized Training Provider

## CONTACT

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