Vitis™ High Level Synthesis

2 days - 14 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Describe the high-level synthesis flow, use the Vitis HLS tool for a first project and identify the importance of the test bench
  - 2 - Use directives to improve performance and area and select RTL interfaces
  - 3 - Identify common coding pitfalls as well as methods for improving code for RTL/hardware
  - 4 - Perform system-level integration of IP generated by the Vitis HLS tool

PREREQUISITES

- C or C++ knowledge
- Basic knowledge FPGAs architectures

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 03/08/2023

CHAPTERS

DAY 1

- Objective 1
  - Introduction to High-Level Synthesis {Lecture}
  - Vitis HLS Tool Flow {Lecture, Lab}
  - Vitis HLS Tool Command Line Interface {Lecture, Lab}
  - Introduction to HLS UltraFast Design Methodology {Lecture}
- Objective 2
  - Design Exploration with Directives {Lecture}
  - Introduction to I/O Interfaces {Lecture}
  - Block-Level I/O Protocols {Lecture, Lab}
  - Port-Level I/O Protocols {Lecture, Lab}
  - Port-Level I/O Protocols: AXI4 Interfaces {Lecture}
  - Port-Level I/O Protocols: Memory Interfaces {Lecture, Lab}
  - Pipeline for Performance: PIPELINE {Lecture, Lab}

DAY 2

- Objective 2
  - Pipeline for Performance: DATAFLOW {Lecture, Lab}
  - Optimizing Structures for Performance {Lecture, Lab}
- Objective 3
  - Vitis HLS Tool Default Behavior: Latency {Lecture}
  - Reducing Latency {Lecture}
  - Improving Area and Resource Utilization {Lecture, Lab}
  - Vitis HLS Tool C Libraries: Arbitrary Precision {Lecture, Lab}
  - Hardware Modeling {Lecture}
  - Using Pointers in the Vitis HLS Tool {Lecture}
- Objective 4
  - HLS Design Flow – System Integration {Lecture, Lab}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vitis 2022.2
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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