Essential DSP implementation techniques for Xilinx™ FPGAs

2 days - 14 hours

OBJECTIVES

- Describe the advantages of using FPGAs over traditional processors for DSP designs
- Utilize fixed point binary arithmetic and identify how to use this knowledge to create efficient designs in FPGAs
- Recognize how both the CLB slices in FPGAs and the more advanced DSP48s are used to implement DSP algorithms
- Explain the dataflow through the device and how to use distributed memory, block RAM, registers, and SRLs to properly implement these designs
- Construct different FIR filter and FFT implementations and how to optimize these implementations in the FPGA

RELATED TRAININGS

- Vitis™ High Level Synthesis
- Designing with the Xilinx™ 7-Series Families
- Designing with the Xilinx™ UltraScale and UltraScale+ Families

PREREQUISITES

- Fundamental understanding of digital signal processing theory and an appreciation of the principles of the following :
  - Sample rates
  - FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filters
  - Oscillators and Mixers
  - FFT (Fast Fourier Transform) algorithm

PARTNERS

XILINX | Authorized Training Provider

CONFIGURATIONS

- No computer is necessary. Only a pencil, eraser and calculator are necessary.

CHAPTERS

1ST DAY

- Back to Basic
  - Traditional DSP vs. FPGA
  - Digital Signal Processing: What, Why, and Where
  - Signed Binary Number Refresher
  - Signed Number Arithmetic
  - Quantization, Saturation, Truncation, and Rounding
  - Latency vs. Throughput
- FPGA Architecture
  - 7 Series Families Overview
  - CLB Structure
  - DSP48E1
  - Block RAM Memory Resources
- FPGA Math
  - Addition and Subtraction
  - Accumulation
  - Multiplication
  - IP Support and Inference
  - Lab
- Shift Registers, RAM and Applications
  - SRL32E
  - Distributed Memory
  - Block Memory
  - Lab
- The FIR Filter
  - Overview
  - MAC Engine FIR
  - Semi Parallel FIR
  - Full Parallel FIR
  - Distributed Arithmetic FIR
  - Inference and IP
  - Lab

2ND DAY

- Advanced Filter Techniques
  - Overview
  - Multiple-Channel Filter
  - Halfband and Interpolated Filters
  - Multiple-Rate Filter: Interpolation Theory
  - Multiple-Rate Filter: Decimation Theory
  - Multiple-Channel, Multiple-Rate Filter
  - Other Functions and Filters
  - Lab
- The Fast Fourier Transform
  - Overview
  - FFT Design
  - FFT Core
  - Lab

TEACHING METHODS

- Classroom training:
  - Face to face
  - Presentation by video projector
  - Provision of PDF course materials
- Virtual training:
  - Onlive training
  - Presentation by Webex
  - Provision of PDF course materials

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
    - Technical questionnaire
    - Result of the Practical Works
    - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics

CONTACT

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