Designing with Xilinx Serial Transceivers

2 days - 14 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Describe and utilize the ports and attributes of the serial transceivers in the UltraScale FPGAs
  - 2 - Use the UltraScale FPGAs Transceivers Wizard to instantiate GT primitives in a design
  - 3 - Effectively utilize the coding, pre-emphasis and linear equalization features of the gigabit transceivers
  - 4 - Use the IBERT design to verify transceiver links on real hardware
  - 5 - Access reference material and debugging tools for your designs

PREREQUISITES

- Verilog or VHDL experience
- Basic knowledge of FPGA architecture and Xilinx implementation tools is helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 13/12/2021

CHAPTERS

DAY 1

- Objective 1
  - UltraScale, UltraScale+, Zynq UltraScale+ Transceivers Overview {Lecture}
  - UltraScale, UltraScale+, Zynq UltraScale+ Transceivers Clocking and Resets {Lecture}
- Objective 2
  - Transceiver Wizard Overview {Lecture, Lab}
  - Transceiver Simulation {Lecture, Lab}
  - Transceiver Implementation {Lecture, Lab}

DAY 2

- Objective 3
  - PCS Layer General Functionality {Lecture}
  - PCS Layer Encoding {Lecture, Lab}
- Objective 4
  - PMA Layer Details {Lecture}
  - PMA Layer Optimization {Lecture, Lab}
- Objective 5
  - Transceiver Test and Debugging {Lecture}
  - Transceiver Board Design Considerations {Lecture}
  - Transceiver Application Examples {Lecture}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

XILINX | Authorized Training Provider

CONTACT

Administratif : +33 (0)6 30 94 50 17
Formateur : +33 (0)6 74 52 37 89
info@mvd-training.com

DATADOCKÉ