Quick Start : Designing with AMD Versal™ Adaptive SoC (French Language) 9h - 17h CET

1 day - 7 hours

OBJECTIVES

- During the event, you'll be introduced to the new AMD Versal™ platform. Explore the heterogeneous Versal™ adaptive SoC architecture containing programmable network-on-chip (NoC) and AI engines, and learn how to use different design tool flows targeting Versal devices.

PREREQUISITES

- Comfort with the C/C++ programming language
- Vitis™ IDE software development flow
- Hardware development flow with the Vivado™ Design Suite
- Basic knowledge of UltraScale™/UltraScale+™ FPGAs and Zynq™ UltraScale+ MPSoCs

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 01/02/202420/07/2023

CHAPTERS

DAY 1

- Architecture Overview {Lecture}
- Design Tool Flow {Lecture, Demo}
- Embedded Software Development {Lecture, Demo}
- NoC Introduction and Concepts {Lecture, Demo}
- AI Engine {Lecture, Demo}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
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SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Recommended display resolution 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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info@mvd-training.com

Qualiopi processus certifié
RÉPUBLIQUE FRANÇAISE
La certification a été délivrée au titre de la catégorie d'action suivante :
ACTIONS DE FORMATION