

Accelerating Applications with the Vitis Unified Environment Software

3 days - 21 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
 - 1 - Explain how the Vitis unified software environment helps software developers
 - 2 - Describe how the FPGA architecture lends itself to parallel computing, as well as the ALVEO boards
 - 3 - Describe the Vitis execution model (OpenCL API)
 - 4 - Profile the design using the Vitis analysis tool
 - 5 - Create kernels from C, C++ or RTL IP using the RTL kernel creation wizard
 - 6 - Apply host code and kernel optimization techniques
 - 7 - Describe existing libraries and create an extensible platform

PREREQUISITES

- Basic knowledge of Xilinx FPGA architecture
- Comfort with the C/C++ programming language
- Software development flow

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.



NOTES

- Release date: 20/12/2021

CHAPTERS

DAY 1

- Objective 1
 - Introduction to the Vitis Unified Software Platform {Lecture}
 - Vitis IDE Tool Overview {Lecture, Labs}
 - Vitis Command Line Flow {Lecture, Labs}
- Objective 2
 - Introduction to Hardware Acceleration {Lecture}
 - Alveo Data Center Accelerator Cards Overview {Lecture}
 - Getting Started with Alveo Data Center Accelerator Cards {Lecture}

DAY 2

- Objective 3
 - Vitis Execution Model and XRT {Lecture, Labs}
 - Synchronization {Lecture, Lab}
 - NDRanges {Lecture}

- Objective 4
 - Profiling {Lecture}
 - Debugging {Lecture}
- Objective 5
 - Introduction to C/C++ based Kernels {Lecture, Lab}

DAY 3

- Objective 5
 - Using the RTL Kernel Wizard to Reuse Existing IP as Accelerators {Lecture, Lab}
- Objective 6
 - Optimization Methodology {Lecture}
 - C/C++ based Kernel Optimization {Lecture}
 - Host Code Optimization {Lecture}
 - Optimizing the Performance of the Design {Lecture, Lab}
- Objective 7
 - Vitis Accelerated Libraries {Lecture}
 - Creating a Vitis Embedded Acceleration Platform (Edge) {Lecture}

TEACHING METHODS

- Inter-company online training :
 - Presentation by Webex by Cisco



- Provision of course material in PDF format
- Labs on Cloud PC by RealVNC



METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
 - Technical questionnaire
 - Result of the Practical Works
 - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
 - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
 - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
 - Expert DSP & RFSoc XILINX - HLS - Matlab - Design DSP RF
 - Expert ACAP XILINX - AI Engines - Heterogenous System Architect

PC RECOMMENDED

- Software Configuration :
 - WebEx Cisco
 - RealVNC Viewer
- Hardware configuration:
 - Vitis unified software platform 2021.1
 - Recent computer (i5 or i7)
 - OS Linux 64-bits
 - At least 16GB RAM
 - Display resolution recommended 1920x1080

PARTNERS



CONTACT

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