Workshop : Designing with the Network On Chip of AMD Versal (French Language) 9h - 17h CET

1 day - 7 hours

OBJECTIVES

- After completing this comprehensive training, you will have the necessary skills to:
  - Identify the major network on chip components in the Versal ACAP
  - Include the necessary components to access the NoC from the PL
  - Configure connection QoS for efficient data movement

PREREQUISITES

- Any Xilinx device architecture class
- Familiarity with the Vivado® Design Suite

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 01/04/2024

CHAPTERS

DAY 1

- NoC Introduction and Concepts
- NoC Architecture
- NoC DDR Memory Controller
- NoC Performance Tuning

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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info@mvd-training.com

Qualiopi processus certifié
RÉPUBLIQUE FRANÇAISE
La certification a été délivrée au titre de la catégorie d'action suivante :
ACTIONS DE FORMATION