Designing with Versal™ AI Engine

4 days - 28 hours

OBJECTIVES

- After completing this comprehensive training, you will have the necessary skills to:
  - Describe the Versal ACAP architecture at a high level
  - Describe the various engines in the Versal ACP device and the motivation behind the AI Engine
  - Describe the architecture of the AI Engine
  - Describe the memory access structure for the AI Engine
  - Describe the full application acceleration flow with the Vitis tool
  - Enumerate the toolchain for Versal AI Engine programming
  - Explain what intrinsic functions are
  - Program a single AI Engine kernel using the XChessDE tool
  - Program multiple AI Engine kernels using static data flow (SDF) graphs
  - Describe the system-level flow, which includes PS + PL + AIE (SW-HW-SW) designs
  - Describe the supported emulation for a system-level design
  - Describe the data movement between the PS, PL, and AI Engines
  - Describe the implementation of the AI Engine core and programmable logic
  - Implement a system-level design for Versal ACAPs with the Vitis tool flow
  - Utilize advanced MAC intrinsic syntax and application-specific intrinsics such as DDS and FFT
  - Utilize the AI Engine DSP library for faster development
  - Apply location constraints on kernels and buffers in the AI Engine array
  - Apply runtime parameters to modify application behavior
  - Debug a system-level design

RELATED TRAININGS

- Designing with the Versal ACAP: Architecture and Methodology
- Designing with the Versal ACAP: Network On Chip

PREREQUISITES

- Comfort with the C/C++ programming language
- Software development flow
- Vitis software for application acceleration development flow

PARTNERS

XILINX | Authorized Training Provider

CONFIGURATIONS

- Software Configuration :
  - Vitis unified software platform 2020.2
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

CHAPTERS

DAY 1

- Overview of Versal ACAP Architecture
- Introduction to the Versal AI Engine Architecture
- Versal AI Engine Memory and Data Movement
- Versal AI Engine Tool Flow
- Application Partitioning on Versal ACAPs
- Data Types: Scalar and Vector Data Types
- Intrinsic Functions

DAY 2

- Window and Streaming Data APIs
- The Programming Model: Single Kernel
- The Programming Model: Introduction to the Data Flow Graph
- The Programming Model: Multiple Kernels Using Graphs

DAY 3

- Application Partitioning on Versal ACAPs
- ACAP Data Communications
- System Design Flow
- Introduction to Advanced Intrinsic Functions

DAY 4

- AI Engine DSP Library Overview
- Advanced Graph Input Specifications
- AI Engine Application Debug and Trace

TEACHING METHODS

- Classroom training:
  - Face to face
  - Presentation by video projector
  - Provision of PDF course materials
- Virtual training:
  - Onlive training
  - Presentation by Webex
  - Provision of PDF course materials

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL

- Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
- Expert SoC & MPSoC XILINX - Language C/C++ - System Design
- Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
- Expert ACAP XILINX – AI Engines – Heteregenous System Architect

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

CONCERNED PUBLIC

- Software and hardware developers, system architects, and anyone who needs to accelerate their software applications using Xilinx devices

CONTACT

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