# Designing with Versal® AI Engine

4 days - 28 hours

## OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Describe the architecture and the memory access structure of the AI Engine
  - 2 - Describe the full application acceleration flow with the Vitis™ tool
  - 3 - Program a single AI Engine kernel using the Vitis IDE tool
  - 4 - Program multiple AI Engine kernels using Adaptive Data Flow (ADF) graphs
  - 5 - Describe the system-level flow, the data movement between the PS, PL, and AI Engines, and the advanced graph input specifications
  - 6 - Implement an AI Engine kernel using intrinsics for a symmetric FIR.
  - 7 - Utilize various AI Engine kernel optimization techniques
  - 8 - Debug an application using the simulation debugging methodology and event traces
  - 9 - Utilize the AI Engine DSP library for faster development

## PREREQUISITES

- Comfort with the C/C++ programming language
- Software development flow
- Vitis software for application acceleration development flow

## CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

## NOTES

- Release date: 20/12/2021

## CHAPTERS

**DAY 1**

- Objective 1
  - Overview of Versal ACAP Architecture {Lecture}
  - Introduction to the Versal AI Engine Architecture {Lecture}
  - Versal AI Engine Memory and Data Movement {Lecture}
- Objective 2
  - Versal AI Engine Tool Flow {Lecture, Lab}
  - Application Partitioning on Versal ACAPs {Lecture}
- Objective 3
  - Data Types: Scalar and Vector Data Types {Lecture}
  - Intrinsic Functions {Lecture}

**DAY 2**

- Objective 3
  - Window and Streaming Data APIs {Lecture}
  - The Programming Model: Single Kernel {Lecture, Labs}
- Objective 4
  - The Programming Model: Introduction to the Data Flow Graph {Lecture}
  - The Programming Model: Multiple Kernels Using Graphs {Lecture, Lab}
  - Design Analysis : Vitis Analyzer {Lecture}

**DAY 3**

- Objective 5
  - System Design Flow {Lecture, Lab}
  - ACAP Data Communication {Lectures, Lab}
  - Advanced Graph Input Specifications {Lectures, Lab}
- Objective 6
  - Introduction to Advanced Intrinsic Functions {Lecture}

**DAY 4**

- Objective 6
  - AI Engine Symmetric Filter Implementation {Lecture, Lab}
  - Floating-Point Operations {Lecture}
- Objective 7
  - AIE Kernel Optimization – Compiler Directives {Lecture}
  - AIE Kernel Optimization – Coding Style {Lecture, Lab}
- Objective 8
  - AI Engine Application Debug and Trace {Lectures, Lab}
- Objective 9
  - AI Engine DSP Library Overview {Lecture, Labs}

## TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

## METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

## SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
  - Expert FPGA XILINX - Language VHDL/Verilog - RTL Design
  - Expert SoC & MPSoC XILINX - Language C/C++ - System Design
  - Expert DSP & RFSoC XILINX – HLS - Matlab - Design DSP RF
  - Expert ACAP XILINX – AI Engines – Heteregenous System Architect

## PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vitis 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

## PARTNERS

XILINX | Authorized Training Provider

## CONTACT

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