Zynq™ All Programmable SoC : System Architecture, Hardware and Software Design (3 in 1)

4 days - 28 hours

OBJECTIVES

- After completing this comprehensive training, you will have the necessary skills to:
  - Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
  - Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
  - Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
  - Analyze the tradeoffs and advantages of performing a function in software versus PL
  - Describe the various tools that encompass a Xilinx embedded design
  - Rapidly architect an embedded system containing a MicroBlaze or Cortex-A9 processor using the Vivado IP integrator and Customization Wizard
  - Create and integrate an IP-based processing system component in the Vivado Design Suite
  - Design and add a custom AXI interface-based peripheral to the embedded processing system
  - Implement an effective software design environment for a Xilinx embedded system using the Xilinx SDK tools
  - Write a basic user application (under Standalone or Linux) using the Xilinx Software Development Kit (SDK) and run it on an embedded system platform
  - Use Xilinx debugger tools to troubleshoot user applications
  - Apply software techniques to improve operability
  - Maintain and update software projects with changing hardware

RELATED TRAININGS

- Zynq™ All Programmable SoC : System Architecture
- Zynq™ All Programmable SoC : Embedded Systems Hardware Design
- Zynq™ All Programmable SoC : Embedded Systems Software Design
- Zynq™ All Programmable SoC : Embedded Systems Advanced Hardware Design
- Zynq™ All Programmable SoC : Embedded Systems Advanced Software Design

PREREQUISITES

- Digital system architecture design experience
- Basic understanding of microprocessor and FPGA architecture
- Basic understanding of C programming
- Basic HDL modeling experience

PARTNERS

XILINX. | Authorized Training Provider

CONFIGURATIONS

- Software Configuration :
  - Xilinx Vivado™ Design or System Edition 2017.3
- Hardware configuration:
  - Recent computer (i5 or i7)
  - Windows 7 64b
  - At least 8GB RAM
  - Minimum display resolution 1024 x 768, recommended 1920x1080

CHAPTERS

1ST DAY

- Overview of Embedded Hardware Development
- Embedded UltraFast Design Methodology
- Zynq AP SoC Architecture Overview
- Inside the Application Processor Unit (APU) {Lab}
- Processor Input/Output Peripherals
- Introduction to AXI
- Zynq AP SoC PS/PL AXI Interfaces
- AXI: Connecting AXI IP
- Using the Create and Import Wizard to Create a New AXI IP {Lab}

2ND DAY

- DMA Controller (DMAC) {Lab}
- DMA
  - Introduction and Features
  - Block Design and Interrupts
  - Read and Write
- Zynq booting
- Zynq AP Memory Resources
- Introduction to Interrupts
- Meeting Your Performance Goals
- Debugging the Zynq AP {Lab}
- MicroBlaze Processor Architecture Overview
- Zynq UltraScale+ MPSoC Architecture Overview

3RD DAY

- Overview of Embedded Software Development
- Driving the SDK Tool {Lab}
- System Debugger {Lab}
- Standalone Software Platform Development {Lab}
- Memory File System (Standalone) {Lab}
- Using Linker Scripts {Lab}
- Interrupts: Software Considerations {Lab}

4TH DAY

- Operating Systems: Introduction and Concepts
- Linux: A High-Level Introduction
- Linux Software Application Development Overview {Lab}
- Booting Overview {Lab}
- Profiling Overview {Lab}
- Understanding Device Drivers
- Custom Device Drivers {Lab}

TEACHING METHODS

- Face to face
- Presentation by video projector
- Provision of paper-based course materials

SUPPORT

- Authorized Trainer Provider XILINX : Engineer Electronics and Telecommunications ENSIL
    - Expert FPGA XILINX - Language VHDL - DSP - Design RTL

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
    - Technical questionnaire
    - Result of the Practical Works
    - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics

CONTACT

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